

CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

- 1 1. An integrated circuit including
2 a patterned copper layer,
3 a patterned aluminum layer,
4 a stud connection in an opening between a
5 location on said patterned copper layer and a
6 location on said patterned aluminum layer, and
7 a liner in said opening and extending between
8 said stud connection and said location on said
9 patterned copper layer.
- 1 2. An integrated circuit as recited in claim 1
2 wherein said liner comprises
3 a layer of tantalum nitride, and
4 a layer of PVD tungsten.
- 1 3. An integrated circuit as recited in claim 1
2 wherein said liner comprises
3 a layer of titanium, and
4 a layer of titanium nitride or PVD tungsten.
- 1 4. An integrated circuit as recited in claim 1
2 wherein said stud connection is formed of tungsten.

1 5. An integrated circuit as recited in claim 1
2 wherein said patterned aluminum layer includes a
3 layer of at least one of titanium and titanium
4 nitride.

1 6. An integrated circuit as recited in claim 2
2 wherein said patterned aluminum layer includes a
3 layer of at least one of titanium and titanium
4 nitride.

1 7. An integrated circuit as recited in claim 3
2 wherein said patterned aluminum layer includes a
3 layer of at least one of titanium and titanium
4 nitride.

1 8. An integrated circuit as recited in claim 4
2 wherein said patterned aluminum layer includes a
3 layer of at least one of titanium and titanium
4 nitride.

1 9. An integrated circuit as recited in claim 1,
2 further including a covering layer.

1 10. An integrated circuit as recited in claim 9
2 wherein said covering layer includes a layer of
3 silane-based high density plasma oxide.

- 1 11. A method of forming an interface structure
2 between copper and aluminum metallurgy layers in an
3 integrated circuit, said method comprising steps of
4 covering a copper metallurgy layer with an
5 insulator,
6 forming an opening through said insulator to
7 said copper metallurgy layer,
8 forming a liner of a conductive barrier
9 material in said opening, and
10 filling a remainder of said opening with a
11 conductive material to form a stud, and
12 forming a patterned aluminum metallurgy layer
13 over said stud.
- 1 12. A method as recited in claim 11, wherein said
2 step of forming a liner includes the further steps
3 of chemical vapor deposition of tantalum nitride and
4 tungsten, respectively.
- 1 13. A method as recited in claim 11, including the
2 further step of
3 forming a covering layer over said patterned
4 aluminum layer.
- 1 14. A method as recited in claim 14, wherein said
2 covering layer includes a layer of silane-based high
3 density plasma oxide.

1 15. A method as recited in claim 11, wherein said
2 patterned aluminum layer includes interconnects and
3 solder or wire bond connection pads, said method
4 including the further step of
5 opening said covering layer at a said solder or
6 wire bond connection pad.

1 16. A method as recited in claim 11, including the
2 further step of forming a barrier layer over said
3 copper metallurgy layer.